REMARKS

Claims 1-9 are pending in the application.

Claims 1, 2 and 4 were rejected under 35 USC 103(a) as being unpatentable over applicant's admitted prior art and Hu, *et al.* (U.S. Pat. No. 5,780,899). This rejection is respectfully traversed.

Claim 1 recites an SRAM comprising MOS transistors, each including "a channel-forming semiconductor region and a gate electrically connected with each other." The Examiner asserts that the prior art shown in Fig. 9 in combination Hu teaches the claimed invention. Fig. 9 of the application shows a conventional SRAM cell. The Examiner asserts that Hu teaches a DTMOS device that has the n-well deeper than the p-well and can be used in CMOS circuitry. See Fig. 7 of Hu.

In Fig. 7, Hu discloses an n-channel dynamic threshold MOSFET. Hu does not, however, disclose that a DTMOS can be used for any of the transistors in a SRAM device. Merely disclosing the structure of a DTMOS device, which was well known in the art at the time of the invention, and reciting that it can be used in a CMOS device is insufficient to support this rejection. There is simply nothing in Hu which suggests using a DTMOS device in a SRAM as claimed. Accordingly, the features of claim 1 are neither taught nor suggested by Hu.

Claims 2 and 4 include additional features related to the selective use of DTMOS transistors in the SRAM. Hu fails to teach or suggest using the DTMOS in a SRAM as stated above, and fails to teach or suggest using DTMOS type transistors for specific transistors within a SRAM. Therefore, the features of claims 2 and 4 are also not taught or suggested by Hu. Accordingly, applicant respectfully requests the withdrawal of the rejection of claims 1, 2 and 4 under 35 USC 103(a) over Fig. 9 of the application in view of Hu.

Claim 3 was rejected under 35 USC 103(a) as being unpatentable over applicant's admitted prior art and Hu and further in view of Tsui *et al.* (U.S. Pat. No. 5,960,289). This rejection is respectfully traversed.

Applicant submits that these 3 references are not properly combinable because there is no motivation or suggestion or teaching within the 3 references to combine these specific references. Furthermore, the combination fails to teach or suggest each and every feature of claim 3. For example, claim 3 recites "said p-type MOS transistor has a gate oxide film larger in thickness than said n-type MOS semiconductor transistor." Claim 3 also depends from claim 2 and includes the features of claim 2, which are not taught by Hu in combination with Fig. 9, nor does Tsui teach or suggest using DTMOS transistors for the specific transistors in the SRAM as claimed. As to the additional feature of claim 3, Tsui fails to teach or disclose the p-type transistor having a gate oxide film larger in thickness than the n-type transistor. Tsui's general disclosure of a dual thickness gate oxide layer falls far short of the specific teaching of using a larger thickness in one of the transistors within a SRAM. Tsui's teaching, even if properly combined, would merely teach using a dual thickness layer for all transistors. Accordingly, applicant respectfully requests withdrawal of the rejection of claim 3 under 35 USC 103(a) in view of Fig. 9, Hu and Tsui.

Claim 5, 6, 8 and 9 were rejected under 35 USC 103(a) as being unpatentable over applicant's admitted prior art in view of Hu and further in view of Hodges, *et al.* This rejection is respectfully traversed.

Rejected claims 5, 6 and 8 depend from claim 1. As stated above, the admitted prior art and Hu are not properly combinable and, even if properly combinable, fail to teach or suggest each and every feature recited in claim 1. Again, applicant submits that the addition of Hodges

to the previous combination is improper because there is no teaching, suggestion or motivation in those 3 references for combining those specific references. Furthermore, the addition of Hodges fails to remedy the deficiencies of the admitted prior art and Hu as related to the features claimed in claim 1. In addition, the specific arrangements of transistors and resistors and the function of these transistors and resistors as claimed in the rejected claims are not taught or suggested by Hodges. Hodges merely teaches a bipolar cellular array where the emitter cells are used to replace the lightly doped n-type silicon from the transistor structure to form diodes. Hodges does not specifically teach or suggest the DTMOS transistor or using resistors within the transistor.

Claim 9 is an independent claim and recites first MOS transistors which each have a channel-forming semiconductor region formed of a first well and second MOS transistors which each have a channel-forming semiconductor region formed of a second well deeper than the first well. None of the prior art references of record teach or suggest this feature.

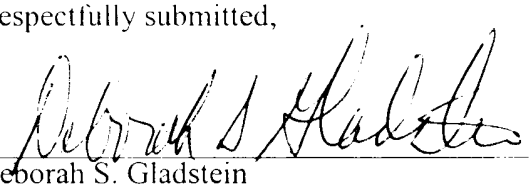
Accordingly, applicants respectfully request withdrawal of the rejection of claims 5, 6, 8 and 9 under 35 USC 103(a) in view of applicant's admitted prior art, Hu and Hodges.

Applicant submits that all pending claims are in condition for allowance, which action is solicited.

In the event that the transmittal letter is separated from this document and the Patent and Trademark Office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge

the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. 03-1952 referencing docket no. 204552016500.

Respectfully submitted,

Dated: August 29, 2002 By: 

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